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VIDICON MODIFICATION STUDY

SPACE SCIENCES LABORATORY
GENERAL ELECTRIC COMPANY
SPACE DIVISION
P. O. BOX 8555
PHILADELPHIA, PA 19101

JULY 1976

FINAL REPORT: JANUARY 1976 - JULY 1976

AIR FORCE ARMAMENT LABORATORY
AIR FORCE SYSTEMS COMMAND • UNITED STATES AIR FORCE
EGLIN AIR FORCE BASE, FLORIDA

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MTF

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Electronic processing was performed on the video output from a standard vidicon camera using sample and hold modules and integrators. The objective of the equipment development was to square up the apparent MTF of the vidicon to compare with that of a CCD imaging device under conditions of low scene contrast. Improvement in resolution of low contrast targets was noted, but was less than expected (2:1).

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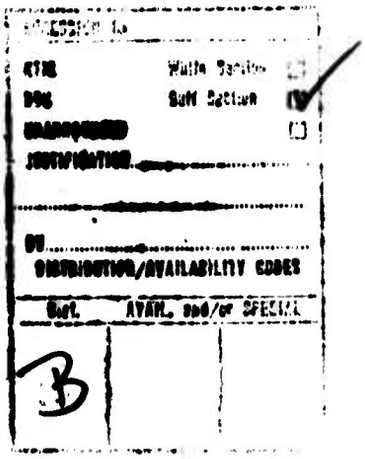
PREFACE

This final report documents the results of the study performed by General Electric Company, Space Sciences Laboratory, P.O. Box 8555, Philadelphia, PA 19101, under Contract Number F08635-76-C-0167 from January through July 1976. This program was sponsored by the Air Force Armament Laboratory, Armament Development and Test Center, Eglin Air Force Base, Florida. The Air Force program manager was CMSgt. Edward B. Hollingsworth, DLMI.

This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

CLIFFORD H. ALLEN, JR., Colonel, USAF
Chief, Guided Weapons Division



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SECTION I

INTRODUCTION

All current armament sensors utilized in the visible spectrum employ vidicon-type imaging tubes which exhibit low resolution factors (modulation transfer function or MTF) when low contrast/high noise level target acquisition is attempted. It had been hypothesized that employing sample/hold circuitry in the post-vidicon electronic processing would provide up to a 2 to 1 increase in resolution of low contrast/high noise level targets.

It was anticipated that the electronic processing would in effect produce a squared up modulation transfer function similar to that produced when a solid state charge transfer device is employed as the imaging device. It was anticipated that the processing electronics would be adaptable to the system by simply taking the video stream from the vidicon, inserting the electronic device, and providing the processed video output to the balance of the video system.

The equipment was designed, constructed, and tested using video tape recordings furnished by the technical contracting officer. Improvement in contrast and resolution was noted where low contrast/high noise signals were present. During the equipment development it was determined that two separate video channels were necessary, one sampling the video signal and integrating it, while the other one was holding and displaying the previously sampled and integrated video signal. The two signal processing chains are effectively flipped back and forth during circuit operation. This technique effectively yields a ratio of sample to hold time of zero, as the output is a continuously held signal which shows no sign of sampling. The sampling goes on during the time the channel is not visible at the output.

Improvement in resolution, when using video tape recordings of actual flights in aircraft, are very difficult to measure quantitatively in that the observer is in effect providing a subjective measurement. Both contractor personnel and the technical contracting officer observed these scenes and noticed improvement in resolution where low contrast/high noise signals were used. Inasmuch as the ultimate use of the system involves personnel observing the low contrast targets, it seemed appropriate to provide the deliverable hardware to Air Force Armament Laboratory (AFATL) for pilot verification of results and further experimentation with the technique.

SECTION II

GENERAL SYSTEM OPERATION

The equipment developed during the Vidicon Modification Study consists of three distinct sections. These are (1) sync and sample pulse generation, (2) timing, and (3) video processing. Refer to Figure 1 for use as a reference in the following discussion.

Six plug-in circuit cards comprise the Vidicon Modification equipment. Cards C1 and C2 are the sync and sample pulse generation cards. The circuitry on these cards is adapted from the SAMPLEDOT narrow bandwidth television processing system. Use of these cards was proposed at the beginning of this contract.

Video from the camera is processed initially in C1-1, as shown in Figure 1. This is a simple 741 operational amplifier which transforms the impedance of the input signal, and signal levels for processing. The output from this stage goes to C1-2, the sync stripper, where both horizontal and vertical sync are removed from the video waveform. The two combined sync signals are then used to trigger C2-1, a one-shot multivibrator. The output pulse from the one-shot forms the reference signal for a voltage controlled oscillator (VCO), divider network, and phase detector. The VCO and phase detector are contained in block C2-2 and the divide by N network is in C2-3 on the block diagram. In this study the VCO, when phase locked, operates at either 8.064 MHz or 6.048 MHz, synchronized to the horizontal and vertical sync pulses. The output of the VCO is also used as an input to a divide by M network included in C2-4. This network is set to a desired division ratio by switches on card C2. Operation of these switches at 8.064 MHz permits 512 or 256 samples per line. When the VCO is operated at 6.048 MHz, switch selection provides either 384 or 192 samples per television line. The output of the M divider generates a sample pulse signal which is fed to card C3. This provides all timing for the video processing circuitry.

The input to C3 consists of a continuous pulse train with 50 percent duty cycle from C2-4, the divide by M network. Output from C3 consists of two signals to command integration or integrator reset in the two video processing channels, and two other signals to command sample or hold in the sample and hold modules on these processing cards. Since the input to the timing card consists of a continuous pulse stream, the output consists of continuous timing commands. It should be noted that these commands also sample the input video during both horizontal and vertical sync pulses. This has no effect on the output signal as the H+V sync is added directly to the processed signal as shown by the interconnection from C1-2 (the H+V sync output from the sync stripper) to C6-2 (the DC offset/sync adder stage).

Figure 2 shows the input and related outputs from the timing circuitry. The sample pulse output from C2-4 is a square wave with 50 percent duty cycle as explained previously. This signal triggers one-shot multivibrators which produce the A channel reset/integrate and sample/hold signals, the B channel reset/integrate and sample/hold signals, and also determines selection of channel A or channel B data. In Figure 2, it is noted that shortly after the

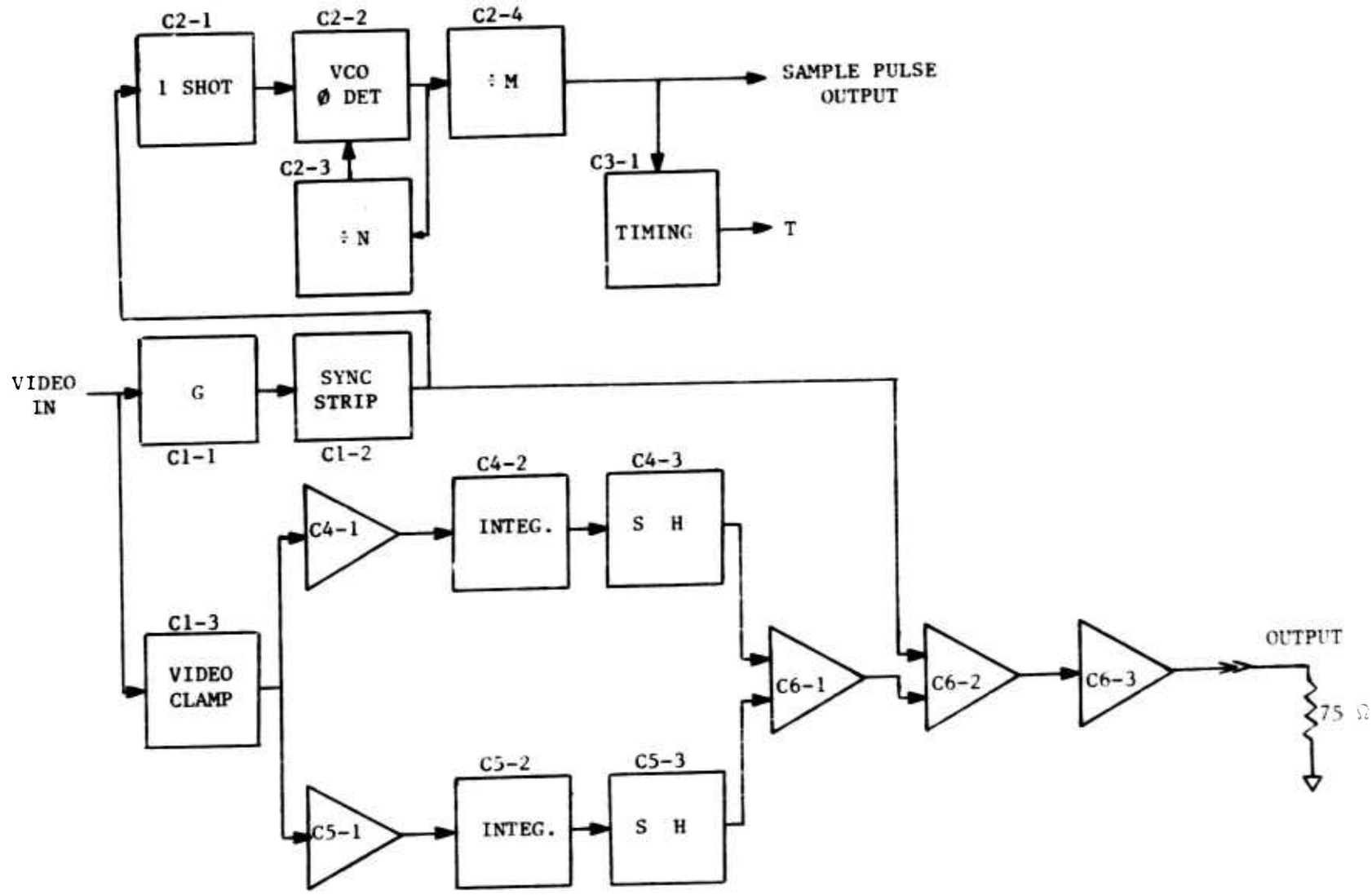

Figure 1. Vidicon Modification Block Diagram

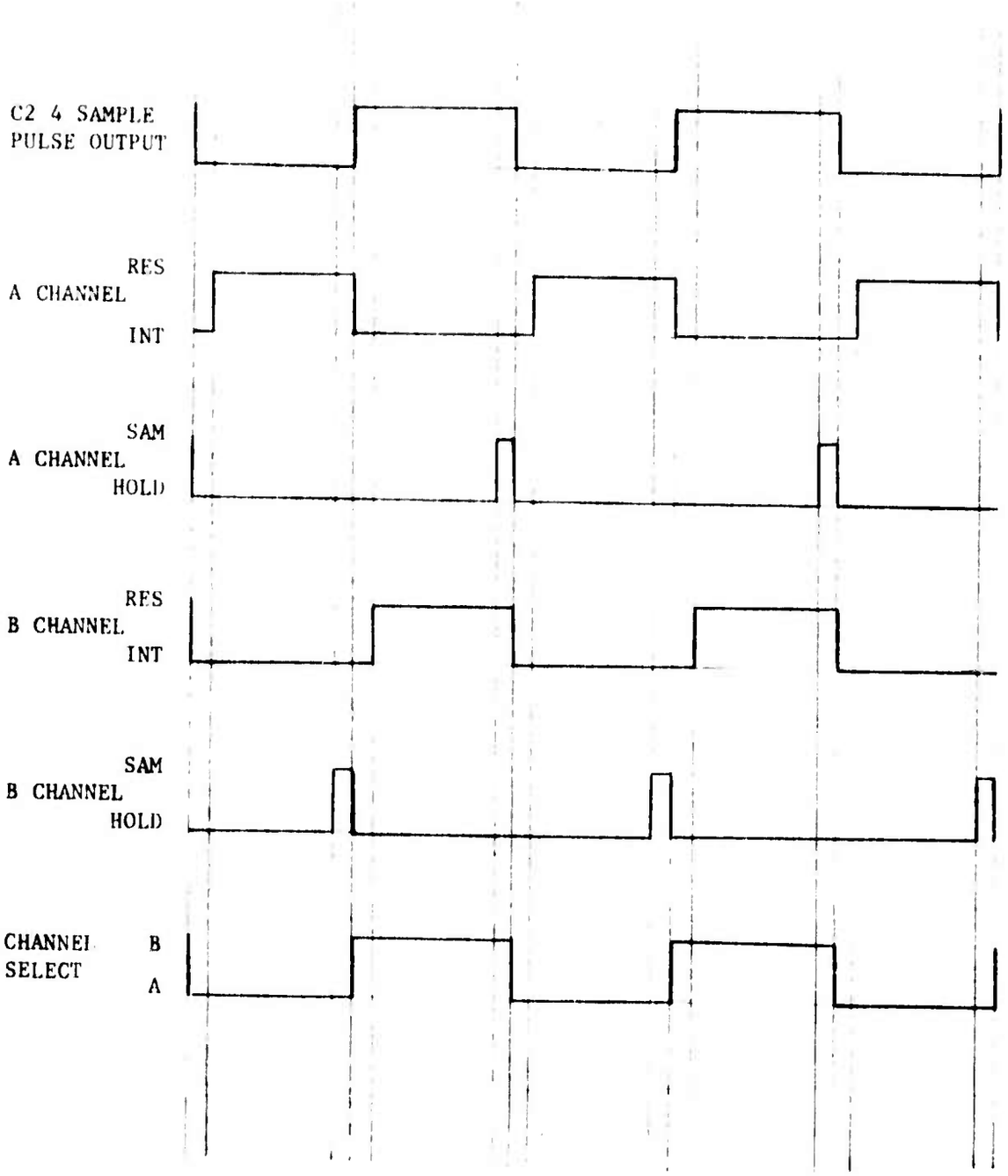

Figure 2. Timing Relationships

A channel sample pulse goes high, the A channel integrator control goes high commanding integrator reset. The integrator switches to integrate mode when the sample pulse output goes to high level. At this point in time the integrator is completely reset and integration of the video input signal for the A channel begins. Near the end of the high portion of the sample pulse, the A channel sample and hold switches from hold to sample. The sample and hold module samples the output of the integrator until the falling edge of the sample pulse output from C2-4. At this point in time the sample and hold switches to hold mode, and channel A output is selected. This causes the now held output from the A channel sample and hold to be presented at the output. As the above is occurring, the B channel circuitry in C5-1, 2, and 3 follow an identical pattern displaced 180 degrees in time, as referenced to the sample pulse output. In this fashion, the held outputs from the A and B sample and hold are switched to the output stages. As one channel is being presented to the output stages, the other channel begins at its integration/sample and hold cycle. At the instant of time that the second channel is presented to the output circuitry, the first channel begins its integration and storage time period.

The timing signals from the above are relatively easy to follow, and they simply provide controls to the integrators and sample and hold modules in the video processing circuitry.

The third area of basic circuitry is video processing. Input video is clamped to ground in C1-3 and then fed directly to the inputs of C4-1 and C5-1. These two amplifiers are high gain-bandwidth product video op amps which drive a storage capacitor to provide the input signal integration. The integrator in each case is represented as block C4-2 and C5-2. Included in each of the integrators is a reset circuit using a 2N709 transistor across the integrating capacitor. This transistor provides a short time constant, short-circuit path for the energy stored in the capacitor. The output of the integrator passes to the sample and hold modules labeled C4-3 and C5-3 in Figure 1. These units are commercially purchased and are Burr-Brown Model SHM-60. They have extremely short aperture times and long retention when commanded into the hold mode. Output signals from the sample and hold go to C6-1, which is a dual input gated video amplifier. The integrated circuit used is the Motorola 1445L. The channel select signal from the timing circuitry determines which of the two inputs to C6-1 are presented at its output. C6-2 adds horizontal and vertical sync to the processed video waveform, and provides the capability to adjust the overall DC and video level of the output signal. This capability permits adjustment of sync level from the nominal 0.3 volt negative-going standard to any other value which may be desired. The output of C6-2 drives a high input-impedance, low output-impedance line driver C6-3 which terminates in 75 ohms. This output is the processed video composite waveform available for use at the monitor.

Summarizing, the sync signal from the incoming video waveform causes a VCO to be phase-locked in frequency. The VCO output is divided down to provide sample pulses which represent X elements on each horizontal video line. The incoming video signal is clamped to ground, integrated and sampled and held alternately in two channels. The output from the sample and hold is selected from a two channel amplifier, sync is read into the composite signal, and the output amplifier provides drive to a 75-ohm load. Connections to the system are relatively easy, consisting of a video input and video output.

SECTION III

SAMPLING AND TIMING

System timing for this equipment consists of generating a signal synchronized with the incoming video, and using it to generate discrete sample intervals. This is accomplished in circuitry shown in block diagram form in Figure 3. The basic operating frequency is generated by the VCO and phase comparator. This integrated circuit, labeled Z1, is an EXAR XR215. The VCO is operated at either 8.064 MHz or 6.048 MHz and drives Z4 a simple inverter, and the Z2, Z3 divider chain. Z2A divides the incoming signal by 8 and supplies $f_o/8$ to Z3. Z3 divides this input by either 8 or 6, depending on the position of the programming switch. The output from Z3 drives Z2B, a divide by 16 counter, which provides one of the two phase comparator inputs for the XR215. The other phase comparator input is derived from card number 1, and is the H+V sync signal from the original video input. Operation of the circuitry consists of the VCO output at a given frequency, and being divided down by Z2A, Z3, Z2B. The output of this divider chain is 7,875 Hz when the VCO is in phase with the incoming video signal. When this is the case, the two phase comparator inputs to the VCO are in synchronism, and no correction results to the VCO output frequency. When the VCO is off frequency however, the output signal from the divider chain will not be in phase synchronization with the H+V sync. This causes an error signal at the output of the phase comparator driving the VCO to the proper frequency.

Z5 is a simple 74121 monostable multivibrator used to generate the sampling pulse output. There are two inputs to this multivibrator, H+V sync and either the output frequency of the VCO or one-half the output frequency of the VCO, as selected. The characteristics of the 74121 are such that when either pin 3 or 4 (the A1 or A2 inputs) are negative going, it will trigger. If the frequency select switch is set at f_o, a sample pulse coinciding with the negative going edge of the VCO output frequency occurs at every cycle of the VCO. If the frequency switch is set at $f_o/2$, a sample pulse results at the output for every other cycle of the VCO. When horizontal or vertical sync pulses occur, the one-shot is triggered and remains triggered until the sync pulse stops. In this fashion sample pulses are generated for the system.

The line rate of a standard video camera is 15,750 Hz which yields 63.492 msec time per TV line. Since sampling occurs in equal intervals over each line, the number of sample pulses per line determines the granularity or resolution of each line. It was earlier indicated that two operating frequencies are used for the VCO. Depending on oscillator frequency, selection of F1 or F2, and selection of the division ratio in Z3, the time per increment and conversely the number of increments per line can be varied. The following table shows both the number of increments per line and time per increment for such combinations.

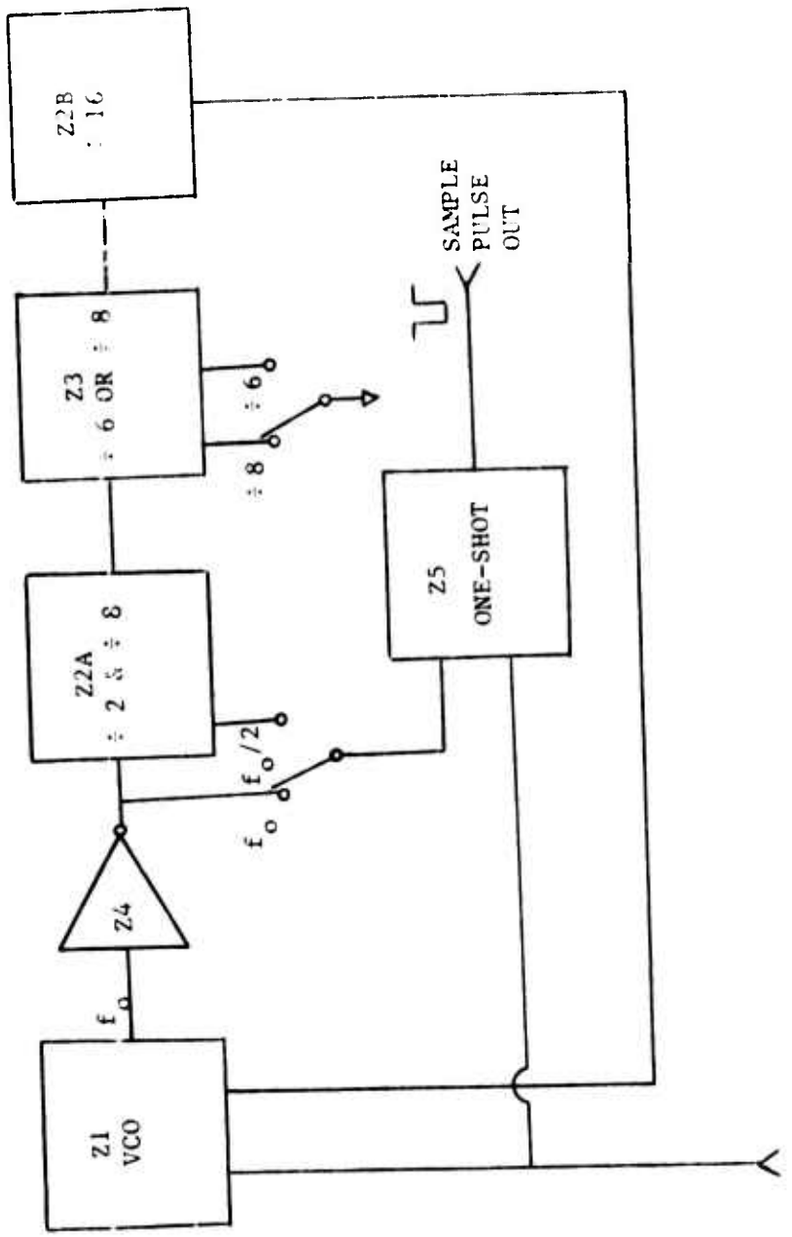

Figure 3. VCO and Divider Block Diagram

Table I. Line Segment Timing

VCO Frequency (MHz)	Sample Pulse Frequency	Z3 : Ratio	Increments Per Line	Time/Line Segment (nsec)
8.064	F1	8	512	124
6.048	F1	6	384	165.4
8.064	F2	8	256	248
6.048	F2	6	192	330.7

It should be noted that the output pulse from Z5 is not the actual width of the video sample. Circuitry following Z5 is a clocked RS flip-flop with the time per line segment being determined by the time interval between successive sample pulse pulses. The pulse width adjustment on Z5 is set to 40 or 50 nsec, which is sufficient to insure triggering the succeeding TTL stages.

During testing of the equipment, it was determined that sampling at 330.7, 248 and 165.4 nsec per line segment produced satisfactory operation. Operation at 124 nsec per line segment was not acceptable due to degradation of the image at the output. Changes in circuit card layout and the method used for resetting the integration circuitry resulted in satisfactory operation at the 124 nsec per line segment rate in the delivered hardware. This corresponds to 512 horizontal increments per line, which is adequate in terms of resolution.

SECTION IV

CONTRAST ENHANCEMENT TESTING

Following design, construction, and debugging of the vidicon modification electronics, a circuit performance evaluation program was conducted. This program covered two areas -- the first being resolution tests using a standard resolution chart, and the second using video tape recordings of low contrast targets taken during test flights. These video tapes were supplied by the contract monitor, and appear to have been made from a helicopter.

Resolution testing was performed using a General Electric 4T321A4A camera which had been fitted with a silicon target vidicon tube. This camera measured 850 TV lines resolution on a laboratory display monitor using the 1956 RETMA Television Resolution Chart as the vidicon camera input. Using the same test setup, but processing the video through the vidicon modification electronics, resolution was measured at 350 TV lines. This degradation is due to the electronic sampling used. There are a discreet number of line elements in each horizontal line, and resolution is directly related to the number of line segments.

The resolution test chart used in the laboratory also provided measurement of resolution with decreasing contrast. The decreasing contrast was simulated by gradually stopping down the vidicon camera lens, effectively lowering the contrast of the video signal. Figure 4 illustrates the results of this testing. For normal video processing, the resolution of the standard test chart was measured by four observers, and their results were averaged to the data given in the figure. This shows 850 TV line resolution for F1.4 varying to 410 TV lines at F8. This is as would be expected; contrast diminishes as the F stop is increased and noise from the electronics and vidicon becomes more predominant with this signal loss. At about F8, a drastic reduction in horizontal resolution became apparent. It is suspected that at this point the electronic noise approaches the signal amplitude, greatly reducing apparent resolution. The second curve on the figure shows resolution measurements by the same four people after the vidicon modification electronics has processed the video signal. It is noted that resolution was degraded significantly at the higher contrast levels, but was improved somewhat at lower contrast levels. The area between the two curves beyond F8.2 is the area of effective contrast enhancement obtained by video processing.

Figure 5 illustrates the relative signal amplitudes which comprise a composite video line. The basic elements are a 0.3 V peak-to-peak pulse which is the line synchronization pulse, a 0.1 V blanking range separating the video signals from the sync pulse, and a 0.6 V peak-to-peak range of video from black to white. A full-contrast scene will produce video signal levels which cover a maximum range of 0.6 V peak-to-peak. Since this range of signal covers the span from whitest white to blackest black, it can be said that a 0.6 V peak-to-peak video signal range represents maximum (i.e., 100 percent) contrast.

Figure 6 graphically shows the reduction in contrast from full-contrast when the camera is stopped down. Full (100 percent) contrast is that which yields a

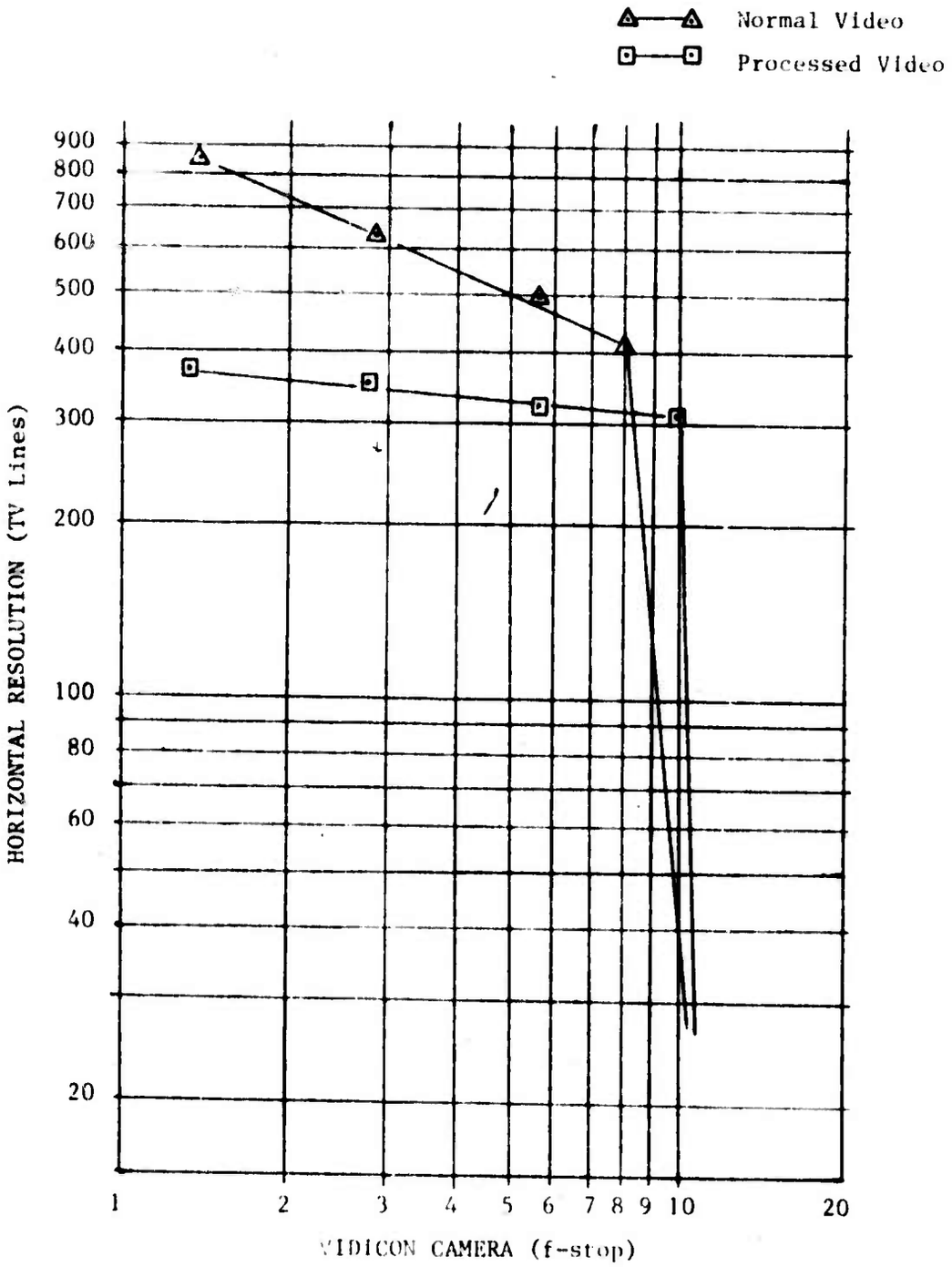

Figure 4. Laboratory Resolution Test Data

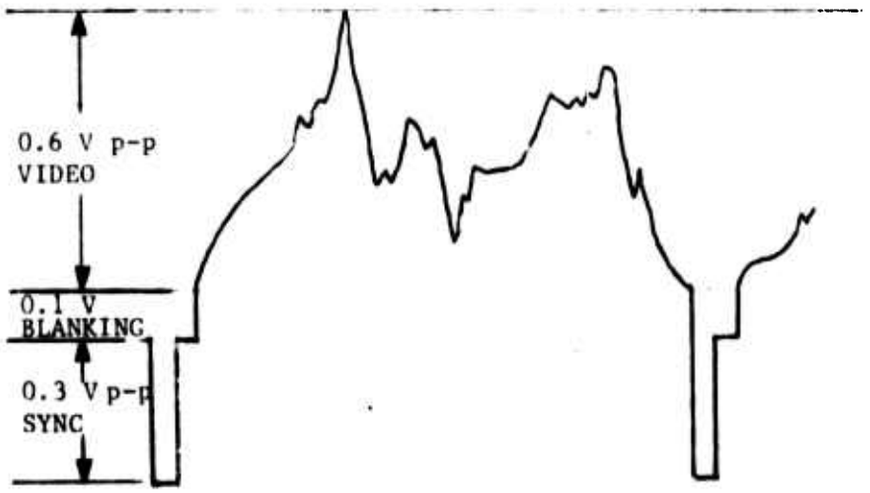

Figure 5. Composite Video Line Signal

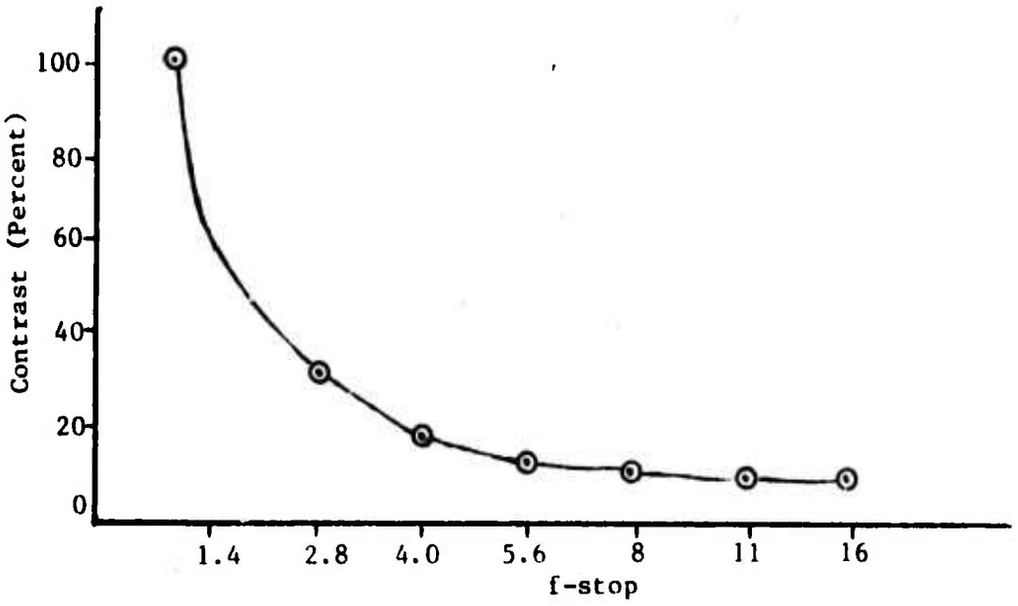

Figure 6. Contrast Reduction by f-stop

video peak-to-peak range of 0.6 volt. Fifty percent contrast is 0.3 volt peak-to-peak.

It was noted during testing, and during adjustment of the equipment after delivery to AFATL that timing of the sample and hold and integrate/reset pulse generators was critical. Very small changes in timing produced significant changes in output resolution, and in the apparent improvement or degradation of contrast. Conclusions relative to this are incorporated in Section V of this report.

Additional subjective evaluation was performed using the video tape recordings supplied by the contract monitor. It was noted that resolution of low contrast scenes from the recordings were improved. The video tape recordings were displayed on laboratory monitors in both unprocessed and processed forms. The monitors were located side by side on a laboratory bench permitting observation of both the processed and unprocessed images. Initial setup consisted of feeding the same video signal to both monitors, and adjusting their brightness and contrast to present identical images to the viewer. The input to the second monitor was then connected to the processed output, and the video recording was observed. In cases where poor light conditions existed or where long slant range provided a long atmospheric path, low contrast was encountered. It was noted that contrast areas such as edges of buildings, junctions of roads, outlines of aircraft on the ground, and outlines of the aircraft being tracked were enhanced somewhat. It was difficult to note contrast enhancement on the airplane being tracked in most cases, as a cross hair was superimposed on the image and the observer was somewhat uncertain as to whether he was viewing a plane or not, since it was covered by the cross hair.

It is felt that the results of the testing of the video tape recordings are more meaningful than those using the standard resolution charts. The actual mission for this equipment is to enhance contrast for either the observer or the tracking electronics on actual flights while attempting to track a flying target or a fixed point on the ground, such as a bridge abutment, etc. Precise measurements of contrast improvement were not possible in this case, due to the subjectivity of the measurement being performed. It is felt advisable to continue the testing program at AFATL using actual flight personnel who are in a better position to indicate whether an improvement is apparent or not. The results of the laboratory testing did indicate an improvement in contrast using the processing electronics albeit a small one.

SECTION V

FUTURE EFFORT

Four areas suggest themselves for future activity with the vidicon modification electronics. These are: 1) timing and adjustment of timing, 2) automatic gamma range adjustment, 3) three or four channel integrate/sample/hold processing, and 4) mechanical layout. Each is covered in a paragraph below.

Timing adjustments were shown to be critical in the developmental activity. System timing for both the sample and hold and the integrate/reset commands were all individually adjustable. This permitted ease in experimentation and familiarization with the various timing adjustments on the laboratory bench. After additional laboratory evaluation, especially by flight personnel who would be using the equipment in the field, it is reasonable to assume that self-adjusting, self-synchronizing timing would be developed and incorporated in the equipment. This, plus the elimination of level adjustment potentiometers, would be quite worthwhile for a field system.

A second area for future work is automatic gamma range adjustment. This process would evaluate each data frame, select the blackest black level and the whitest white level, and automatically adjust the gain of the processing electronics so the blackest black at the input would produce black at the output. The whitest white at the input would likewise produce white at the output. This is another form of contrast enhancement, in that a low contrast scene does not normally take advantage of the full dynamic range from black to white. The circuitry to automatically achieve this would increase contrast for such scenes.

A third area of future endeavor is the use of three or four channel integrate/sample/hold circuitry. It was observed in initial laboratory tests that switching transients, when switching from A channel to B channel appear in the output waveform. These transients are a very short time duration however, and contribute very little to distortion of the output waveform. The settling time at the sample and hold module does influence the output waveform significantly when large transitions occur between subsequent samples of the input video. What happens is the sample and hold module requires a finite amount of time to reach an output level within 0.1 percent of the input value. This time is dependent upon the previously obtained output level, and the new input value. When one has a large differential between the previous value and the current input level, greater time is required for stabilization. The addition of one or two more processing channels would provide additional time for the stabilization of each sample and hold before it is switched to the output. Addition of this circuitry should decrease noise and improve the contrast at the areas of the scene where contrast differentials exist.

The fourth area of future investigation concerns mechanical configuration of the equipment. The delivered hardware is intended for laboratory use and no special pains were taken to provide compactness. The six circuit cards could easily be reduced to three by careful layout. Additional compacting of the physical size can take place by incorporating hybrid microcircuits. As an example, all of the system timing could be reduced to a single hybrid micro[illegible]

requiring a board space of approximately 3/4 x 1 inch. On the laboratory model an entire card was required for this function.

SECTION VI

CONCLUSIONS

Four statements can be made as a result of this program. These conclusions are:

(1) The vidicon modification concept has been verified.

(2) Contrast enhancement after processing by the vidicon modification electronics is apparent.

(3) Actual results (contrast enhancement) appear less than had been predicted, i.e., a 2:1 improvement in contrast was not achieved.

(4) System timing is critical and further development is required in this area.

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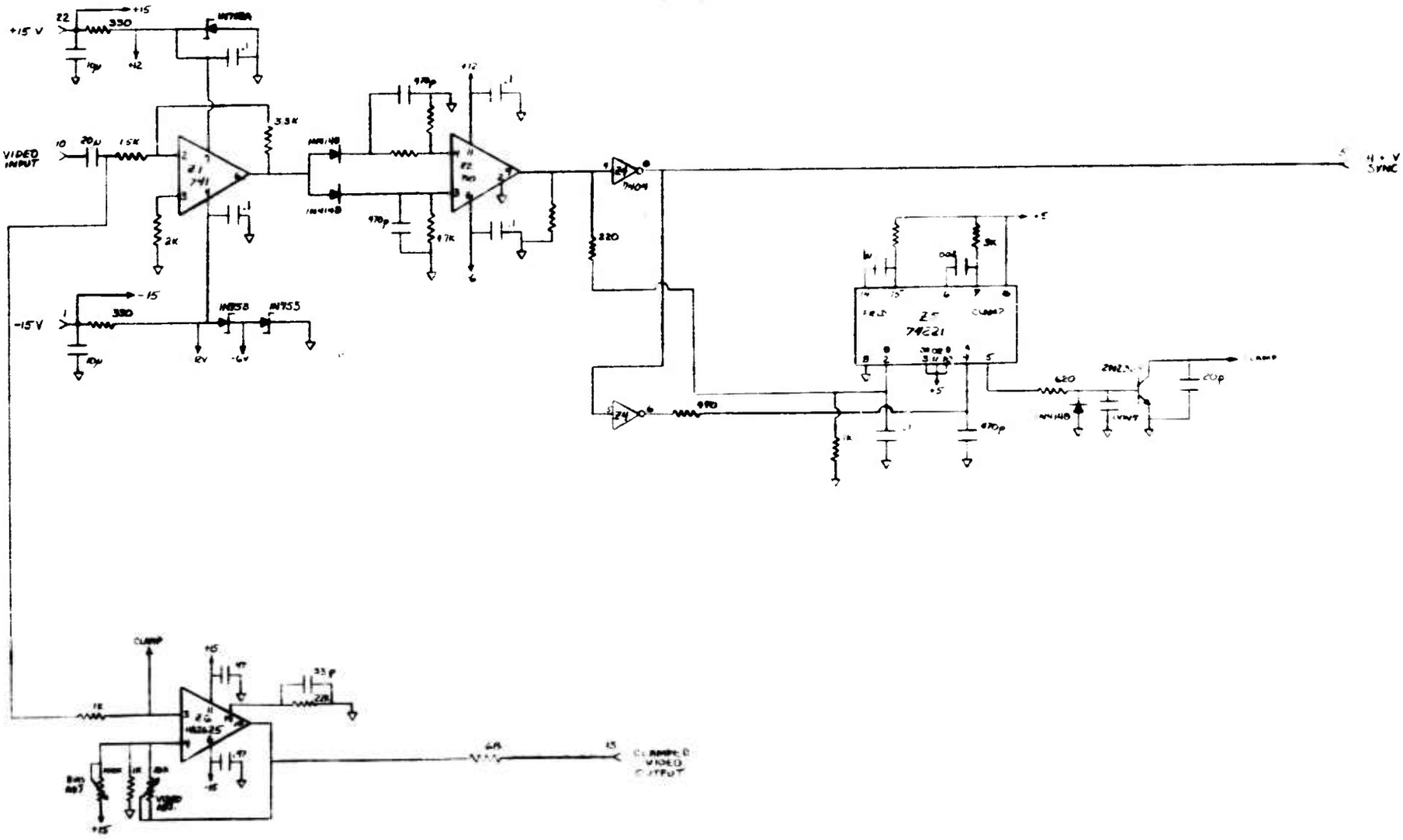
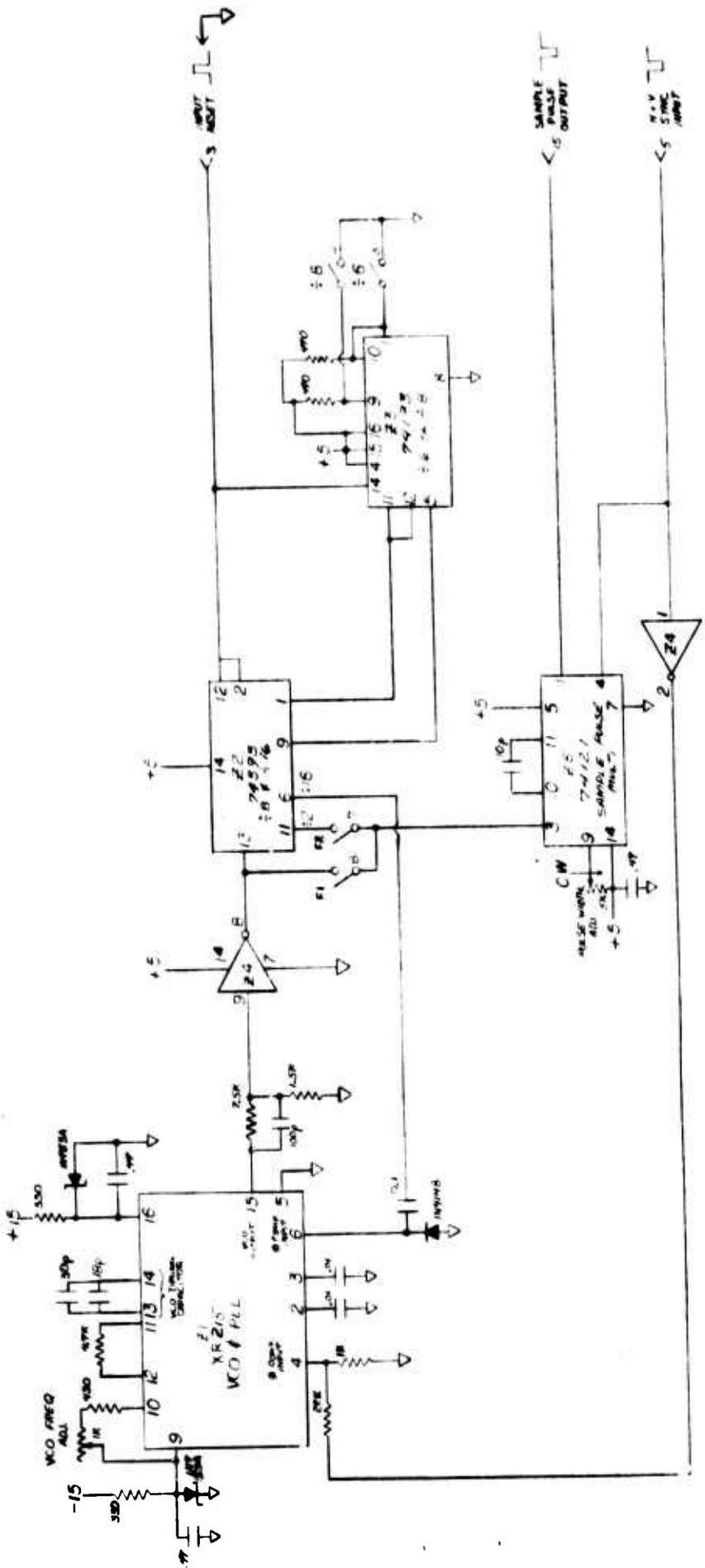
APPENDIX

SCHEMATIC DIAGRAMS



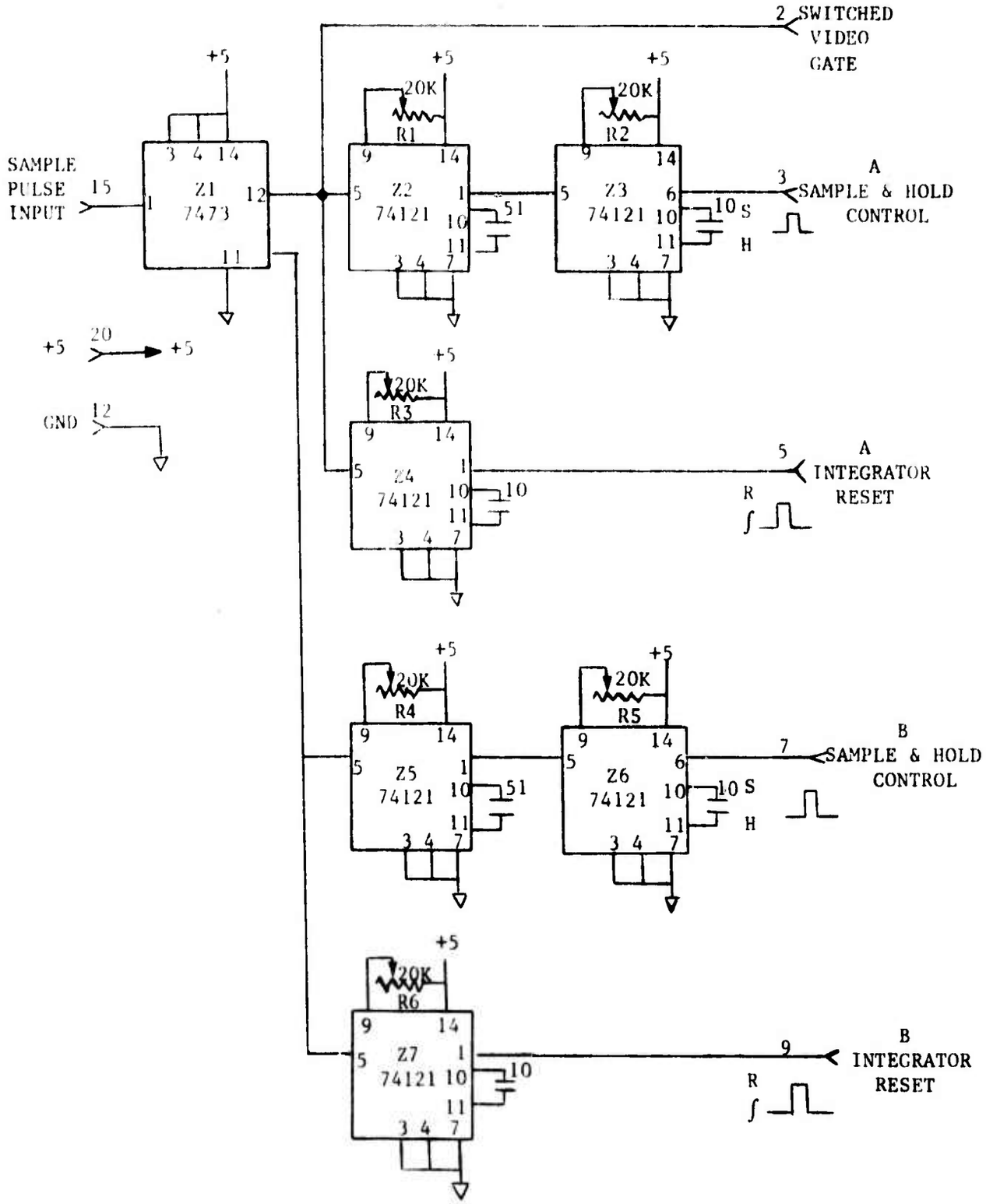
Video and Timing

Card 1



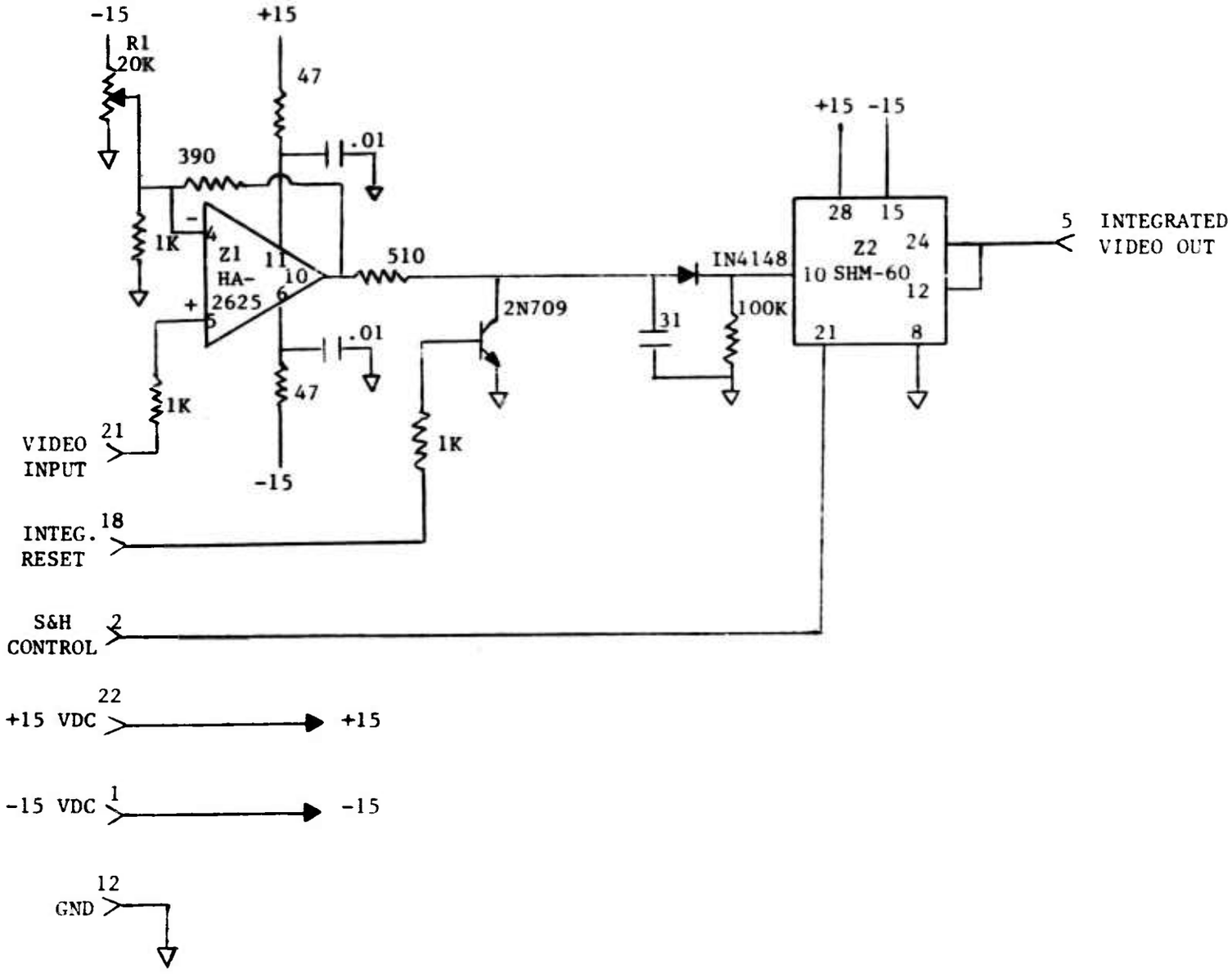
VCO and Divider

Card 2

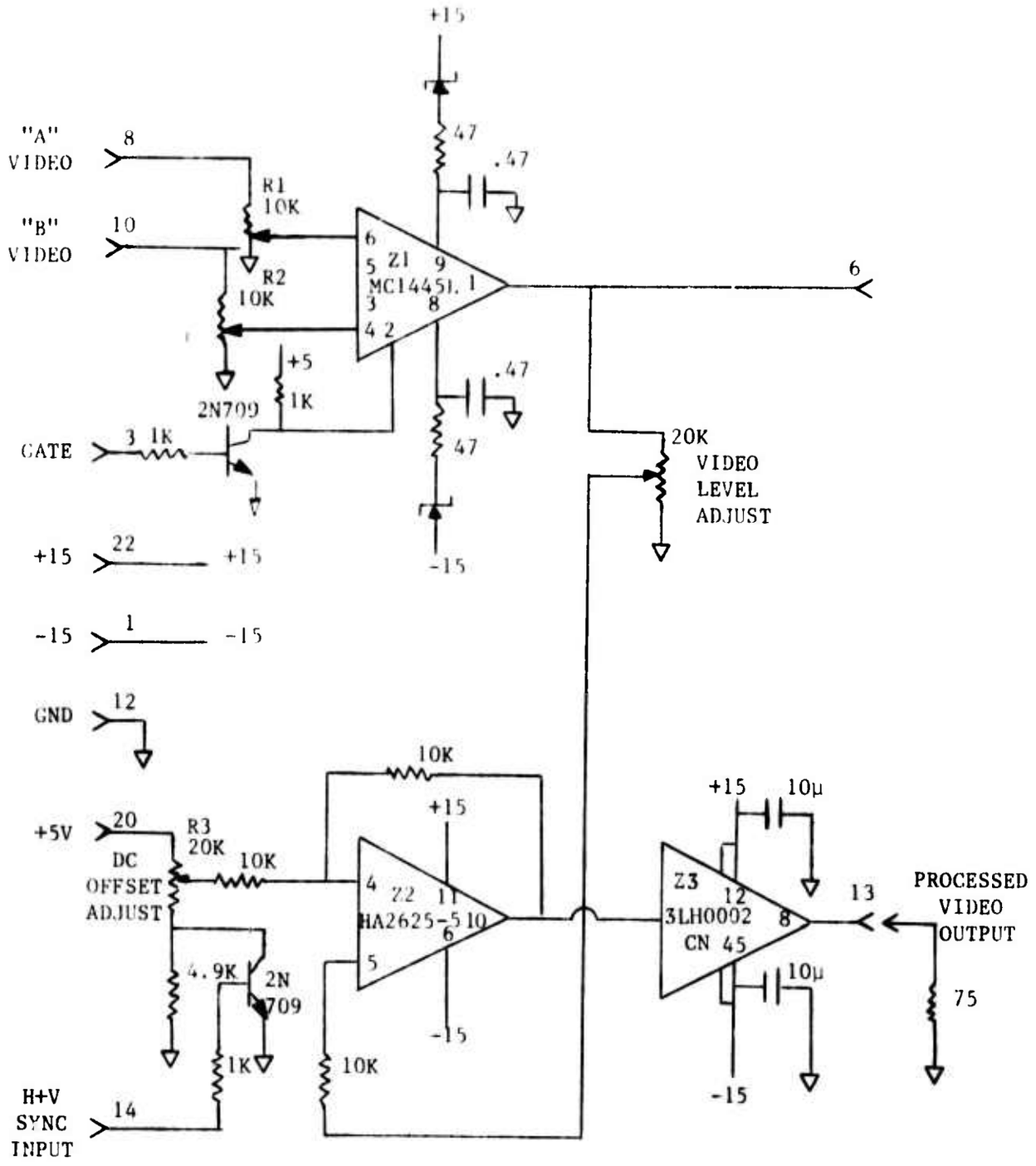


S&H and Integrator Timing

Card 3



Integrator/S&H
Cards 4,5



Video Selector - Sync Adder
Card 6

INITIAL DISTRIBUTION

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